CLAIMS

We claim:

1. A delay element comprising:

an amplifier adapted to receive input signals;

a filter coupled to the amplifier and adapted to provide a variable delay, wherein the filter comprises:

a first inductor having a first terminal and a second terminal, the first terminal coupled to a first output terminal of the amplifier and the second terminal providing a first output signal of the delay element;

a second inductor having a third terminal and a fourth terminal, the third terminal coupled to a second output terminal of the amplifier and the fourth terminal providing a second output signal of the delay element;

at least a first capacitor coupled between the first output terminal of the amplifier and the fourth terminal of the second inductor, wherein a capacitance of the at least first capacitor is variable; and

at least a second capacitor coupled between the second output terminal of the amplifier and the second terminal of the first inductor, wherein a capacitance of the at least second capacitor is variable.

2. The delay element of Claim 1, wherein the filter further comprises:

at least a third capacitor coupled between the fourth terminal of the second inductor and a reference terminal, wherein a capacitance of the at least third capacitor is variable; and

at least a fourth capacitor coupled between the second terminal of the first inductor and the reference terminal, wherein a capacitance of the at least fourth capacitor is variable.

3. The delay element of Claim 2, wherein the reference terminal is at a ground voltage potential.

4. The delay element of Claim 2, wherein the amplifier is a differential amplifier comprising:

a pair of transistors;

a pair of resistors coupled between a supply voltage and corresponding ones of the transistors; and

a current source coupled between the pair of transistors and the reference terminal.

5. The delay element of Claim 2, wherein the at least first and second capacitors each comprises:

a first fixed capacitor;

at least one selectable fifth capacitor coupled in parallel with the first fixed capacitor; and

a first transistor in series with each selectable fifth capacitor and adapted to be controlled to determine whether the associated selectable fifth capacitor is enabled.

6. The delay element of Claim 5, wherein the at least third and fourth capacitors each comprises:

a second fixed capacitor;

at least one selectable sixth capacitor coupled in parallel with the second fixed capacitor; and

a second transistor in series with each selectable sixth capacitor and adapted to be controlled to determine whether the associated selectable sixth capacitor is enabled.

7. The delay element of Claim 2, wherein the delay element is programmable for the variable delay and to account for semiconductor processing variations.

8. The delay element of Claim 2, wherein the filter is an allpass filter and the delay element is adapted to provide an approximately flat magnitude and group delay response across a frequency range.

9. The delay element of Claim 1, wherein the amplifier is a differential amplifier.

10. An equalizer comprising:

a feedforward filter adapted to receive a first input signal and provide a first output signal, wherein the feedforward filter comprises at least one delay element having a variable delay;

an adaptive coefficient generator adapted to receive the first input signal and a second signal and provide tap coefficients to the feedforward filter;

a slicer adapted to receive a slicer input signal and provide a slicer output signal;

a slicer timing alignment block adapted to receive the slicer input signal and provide a second output signal, wherein the slicer output signal is subtracted from the second output signal to generate an error signal;

a tap timing alignment block adapted to receive the slicer output signal and provide a third output signal; and

a first low pass filter adapted to receive the third output signal and the error signal and provide a fourth output signal, wherein the fourth output signal is multiplied with the third output signal to provide a feedback signal which is added to the first output signal to generate the slicer input signal.

11. The equalizer of Claim 10, wherein the delay element comprises:

a first inductor having a first terminal and a second terminal, the first terminal adapted to receive a first delay element signal and the second terminal providing a first delay element output signal of the delay element;

a second inductor having a third terminal and a fourth terminal, the third terminal adapted to receive a second delay element signal and the fourth terminal providing a second delay element output signal of the delay element;

a first capacitor coupled between the first terminal of the first inductor and the fourth terminal of the second inductor, wherein a capacitance of the first capacitor is variable; and

a second capacitor coupled between the third terminal of the second inductor and the second terminal of the first inductor, wherein a capacitance of the second capacitor is variable.

12. The equalizer of Claim 11, wherein the delay element further comprises an amplifier adapted to receive input signals and provide the first delay element signal to the first inductor and the second delay element signal to the second inductor.

13. The equalizer of Claim 12, wherein the delay element further comprises:

a third capacitor coupled between the fourth terminal of the second inductor and a reference terminal, wherein a capacitance of the third capacitor is variable; and

a fourth capacitor coupled between the second terminal of the first inductor and the reference terminal, wherein a capacitance of the fourth capacitor is variable.

14. The equalizer of Claim 13, wherein the first and second capacitors each comprises:

a first fixed capacitor;

at least one selectable fifth capacitor coupled in parallel with the first fixed capacitor; and

a first transistor in series with each selectable fifth capacitor and adapted to be controlled to determine whether the associated selectable fifth capacitor is enabled.

15. The equalizer of Claim 14, wherein the third and fourth capacitors each comprises:

a second fixed capacitor;

at least one selectable sixth capacitor coupled in parallel with the second fixed capacitor; and

a second transistor in series with each selectable sixth capacitor and adapted to be controlled to determine whether the associated selectable sixth capacitor is enabled.

16. The equalizer of Claim 10, wherein the adaptive coefficient generator and/or the slicer timing alignment block comprises at least one delay element having a variable delay.

17. The equalizer of Claim 10, wherein the delay element comprises:

an amplifier adapted to receive input signals and provide a first delay element signal and a second delay element signal;

a first and a second inductor in series, wherein the first inductor receives the first delay element signal at a first terminal and the second inductor provides a first delay element output signal at a second terminal;

a first capacitor coupled between the first and second inductor and a reference terminal;

a third and a fourth inductor in series, wherein the third inductor receives the second delay element signal at a third terminal and the fourth inductor provides a second delay element output signal at a fourth terminal;

a second capacitor coupled between the third and fourth inductor and the reference terminal;

a third capacitor coupled to the first terminal and the fourth terminal;

a fourth capacitor coupled to the third terminal and the second terminal;

a fifth capacitor coupled to the second terminal and the reference terminal; and

a sixth capacitor coupled to the fourth terminal and the reference terminal.

18. The equalizer of Claim 17, wherein the third, fourth, fifth, and sixth capacitor are adapted to have a variable capacitance.

19. A method of providing a variable signal delay, the method comprising:

receiving an input signal;

amplifying the input signal to provide an amplified output signal;

passing the amplified output signal through a filter having inductors and cross-coupled capacitors whose capacitance is variable; and

providing an output signal across load capacitors of the filter whose capacitance is variable to provide a desired signal delay.

20. The method of Claim 19, wherein the capacitance of the cross-coupled capacitors is variable to account for semiconductor processing variations.

21. The method of Claim 19, wherein the filter is an allpass filter adapted to provide an approximately constant group delay and magnitude response over a frequency range.

22. A method of providing a signal delay, the method comprising:

providing an amplifier adapted to amplify input signals and provide amplified output signals; and

providing a filter adapted to filter the amplified output signals, the filter having cross-coupled capacitors and load capacitors whose capacitance is variable to provide a selectable signal delay.

23. The method of Claim 22, wherein the capacitance of the cross-coupled capacitors is variable to account for semiconductor processing variations.

24. The method of Claim 22, wherein the filter is an allpass filter adapted to provide an approximately flat magnitude and group delay response across a frequency range.

25. A delay element comprising:

an amplifier adapted to receive input signals and provide a first signal and a second signal;

a first and a second inductor in series, wherein the first inductor receives the first signal at a first terminal and the second inductor provides a first output signal at a second terminal;

a first capacitor coupled between the first and second inductor and a reference terminal;

a third and a fourth inductor in series, wherein the third inductor receives the second signal at a third terminal and the fourth inductor provides a second output signal at a fourth terminal;

a second capacitor coupled between the third and fourth inductor and the reference terminal;

a third capacitor coupled to the first terminal and the fourth terminal;

a fourth capacitor coupled to the third terminal and the second terminal;

a fifth capacitor coupled to the second terminal and the reference terminal; and

a sixth capacitor coupled to the fourth terminal and the reference terminal.

26. The delay element of Claim 25, wherein the third, fourth, fifth, and sixth capacitor are adapted to have a variable capacitance.

27. The delay element of Claim 25, wherein the third, fourth, fifth, and sixth capacitor each comprises a fixed capacitor in parallel with a selectively enabled capacitor.